Transparent or Hidden Transfer Mode:

The µP executes some states during which it floats the address and data buses.

During these states, µP is isolated from the system bus.

The DMAC transfers data between memory and I/O devices during these states. This operation is transparent to µP.

This is the slowest DMA transfer. In this mode, the instruction execution speed of µP is not reduced. But, the transparent DMA requires logic to detect the states when the µP is floating the buses.

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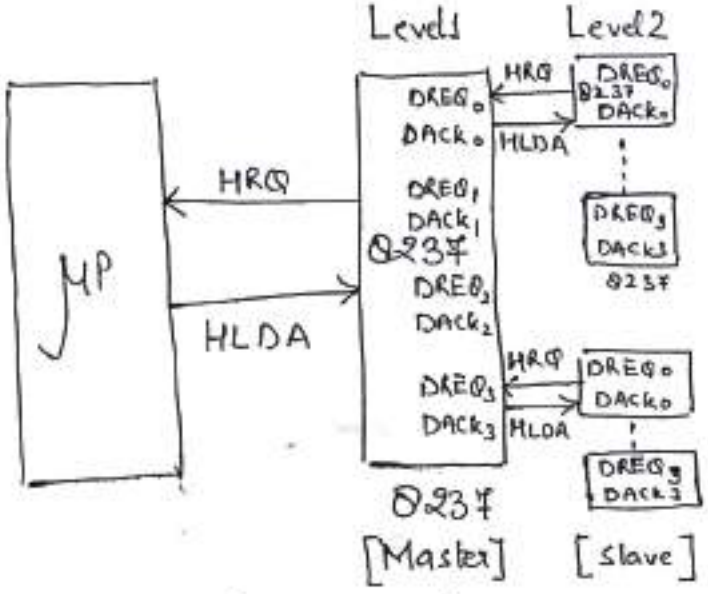
* Single Byte Transfer Mode of DMAC is also known as Cycle stealing Transfer Mode.

There is one more mode used for data transfer through DMAC and that is known as - 'Cascade Mode'. [Also known as master/slave mode]

Cascade Mode :- This mode is used to cascade more than one 8237 together to increase the no. of channels.

The HRQ and HLDA lines of level 2 - 8237 are connected to DREQ and DACK lines of level 1 - 8237 respectively.

Following figure shows cascading of 8237.



Cascaded 8237

and so on.

* There is no limitation of no. of cascading levels.

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Priority :-

8237A has 2 types of priority encoding available as software selectable options.

1. Fixed Priority
2. Rotating Priority

1. **Fixed Priority** :- In the fixed priority, channel 0 has the highest priority and the channel 3 has the lowest priority.

Following figure shows the priority ratings.

	Priority	Channel
Highest →	1	0
	2	1
	3	2
Lowest →	4	3

In the fixed priority, after recognition of any channel to be in service, then the other channels are prevented from interfering with the service until it is completed.

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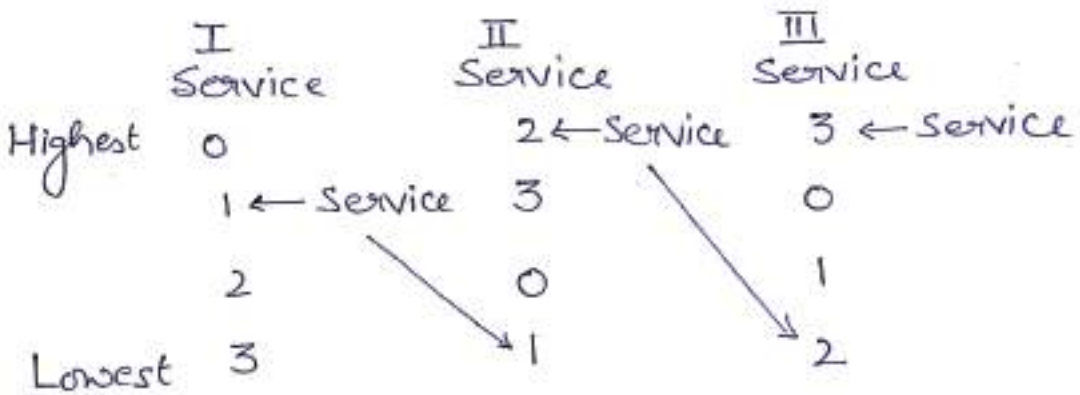
(2) Rotating Priority :- In this, channel being serviced gets the lowest priority and the channel next to ~~its~~ it gets the highest priority, as shown below :-



Rotating Priority

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